Listing of the Claims:

A clean version of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121(c)(3). This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Original) A method of forming a pixellated device, comprising:

defining pixel areas, each pixel area comprising:

a thin film transistor having a gate conductor and source and drain conductors separated by a gate insulator and a semiconductor channel;

a pixel electrode; and

a line conductor associated with the source or drain conductor,

wherein the source and drain conductors, pixel electrodes and line conductors are formed by depositing and patterning a transparent conductor layer and by selectively electroplating areas of the transparent conductor layer to form a metallic layer for reducing the resistivity of the transparent conductor layer, the areas including the line conductors and excluding the source and drain conductors.

2. (Original) A method as claimed in claim 1, wherein the areas also exclude the pixel electrodes.

3. (Previously Presented) A method as claimed in claim 1, wherein the electroplated areas comprise edge regions of the line conductors.

4. (Original) A method of forming a pixellated device, comprising:

defining pixel areas, each pixel area comprising:

a thin film transistor having a gate conductor and source and drain conductors separated by a gate insulator and a semiconductor channel;

a pixel electrode; and

a line conductor associated with the source or drain conductor,

wherein the source and drain conductors, pixel electrodes and line conductors are formed by depositing and patterning a transparent conductor layer and by selectively plating upper surface areas of the transparent conductor layer using an electroless plating step to form a metallic layer for reducing the resistivity of the transparent conductor layer, the areas including the line conductors and excluding the source and drain conductors.

5. (Original) A method as claimed in claim 4, wherein the areas also exclude the pixel electrodes (38).

6. (Original) The method as claimed in any preceding claim, comprising
depositing and patterning a gate conductor layer over an insulating substrate;
depositing a gate insulator layer over the patterned gate conductor layer;
depositing a silicon layer over the gate insulator layer; and
depositing and patterning the transparent conductor layer.

7. (Previously Presented) A method as claimed in claim 1, wherein the selectivity of the plating is achieved using a printed shielding layer.

8. (Original) A method as claimed in claim 7, wherein the selective plating comprises:
printing a shielding layer for shielding the source and drain conductors; and
plating the non-shielded areas of the transparent conductor layer to form a metallic layer for reducing the resistivity of the non-shielded areas.

9. (Original) A method as claimed in claim 7, wherein the selective plating comprises:
plating the transparent conductor layer to form a metallic layer for reducing the resistivity;

printing a shielding layer and removing the metallic layer of the unshielded area.

10. (Previously Presented) A method as claimed in claim 1, wherein the metallic layer comprises copper or silver.

11. (Previously Presented) A method as claimed in claim 1, wherein the transparent conductor layer is pretreated before plating.

12. (Previously Presented) A method as claimed in claim 1, wherein the transparent conductor layer comprises a conductive oxide.

13. (Original) A method as claimed in claim 12, wherein the oxide comprises ITO.

14. (Original) A method as claimed in claim 13, wherein the ITO is deposited by printing.

15. (Previously Presented) A method as claimed in claim 1, wherein the gate conductor is deposited and patterned with a first lithographic process and the transparent conductor layer defining source and drain conductors and pixel electrodes is deposited and patterned with a second lithographic process, the silicon layer being self aligned to the gate conductor.

16. (Previously Presented) A method as claimed in claim 1 for forming the active plate of an active matrix liquid crystal display.

17. (Original) A pixellated device, comprising:
pixel areas, each pixel area comprising:

a thin film transistor having a gate conductor and source and drain conductors separated by a gate insulator and a semiconductor channel;

a pixel electrode; and

a column conductor associated with the source or drain conductor,

wherein the source and drain conductors, the column conductors and the pixel electrodes are defined by a transparent conductor layer having a metallic layer in contact with a portion of the transparent conductor layer, the portion including the column conductors and excluding the source and drain conductors.

18. (Original) A device as claimed in claim 17, wherein the portions also exclude the pixel electrodes.

19. (Previously Presented) A device as claimed in claim 17, comprising:

a gate conductor layer over an insulating substrate defining the gate conductors and also defining row conductors;

the gate insulator layer over the gate conductor layer; and

the silicon layer over the gate insulator layer and defining the semiconductor channel overlying the gate conductors.

20. (Previously Presented) A device as claimed in claim 17 wherein the metallic layer is on top of the portion of the transparent conductor.

21. (Previously Presented) A device as claimed in claim 17, wherein a photoresist layer is on top of the portion of the transparent conductor.

22. (Previously Presented) A device as claimed in claim 17 comprising the active plate of an active matrix liquid crystal display.

23. (Original) An active matrix liquid crystal display comprising an active plate as claimed in claim 22, a passive plate, and a layer of liquid crystal material sandwiched between the active and passive plates.